AN EFFICIENT METHOD OF PMOS STACKED-GATE MEMORY CELL PROGRAMMING UTILIZING FEEDBACK CONTROL OF SUBSTRATE CURRENT

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TECHNICAL FIELD

The present invention provides a method of programming a PMOS stacked-gate memory cell by hot electron injection that utilizes feedback with substrate current. The

15   method allows for an increase of programming effect (V_T shift) and/or a reduction of programming voltage and/or a reduction in drain current.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a partial cross-section drawing illustrating the general structure of a PMOS

20   stacked gate memory cell.

Fig. 2 is a graph showing floating gate current versus floating gate voltage.

Fig. 3 is a graph showing substrate current versus floating gate voltage.

Figs. 4A and 4B are block diagrams illustrating feedback realization using, respectively, the signal from an entire NVM array and from a small reference cell.

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DESCRIPTION OF THE INVENTION

Hot electron injection is a well known and widely used method of programming nonvolatile memory (NVM) cells. It is a common programming mechanism for stacked-gate cells, split-gate cells and other currently available NVM cells.

30   Fig. 1 provides a general schematic representation of a conventional PMOS stacked gate NVM cell 100 formed in an N-type region 102 of semiconductor material, e.g. crystalline silicon. Those skilled in the art will appreciate that the N-type region 102 is typically an n-well formed in a P-type silicon substrate. The PMOS device 100 includes a conductive floating gate (FG) electrode 104, e.g. polysilicon, that is separated from the

N-type region 102 by a layer of thin gate dielectric material 106, e.g. silicon dioxide. A control gate (CG) electrode 108, e.g. polysilicon, is separated from the floating gate 104 by a layer of interpoly dielectric material 110, e.g. an oxide-nitride-oxide sandwich. P-type diffusion regions 112 formed at the sides of the stacked gate structure provide the

5 source/drain regions of the PMOS cell 100 and define an N-type channel region therebetween. The fabrication techniques for making the PMOS device 100 are well known.

When applied to a PMOS based stacked-gate cell 100, the hot electron injection programming method assumes that a high negative voltage is applied to the drain of the PMOS device. Depending on the erasing and coupling coefficient, a corresponding voltage

10 is applied to the control gate 108 that brings the potential of the floating gate 104 to a value that is negative, but lower in absolute value compared with drain. In these conditions, the high lateral electric field creates hot electrons, and the high perpendicular electric field helps the hot electrons to reach the floating gate 104 through thin gate oxide 106. The injection current essentially depends on the potential of the drain and floating gate 104; that is, the

15 more drain voltage, the more injection.

As shown in the Fig. 2 graph of PMOS floating gate current versus floating gate voltage, the gate current of the PMOS device 100 has a maximum with respect to the floating gate voltage. As shown in Figs. 2 and 3, this maximum has the same origin and correlates well with substrate current.

20 With continuing reference to the Fig. 2 graph, conventional programming starts from a floating gate potential that is close to the right side of the pick (position 1 in Fig. 2). During programming, the floating gate 104 receives a negative charge of electron injection current. As a result, the floating gate potential moves to more negative values until it stops in a position 2 (Fig. 2) with very low injection current. This means the end of programming

25 that results in a shift of V_T that is equal to the voltage difference (Delta) between positions 1 and 2. This shift depends on the drain voltage via the pick's width; it does not depend on pick's height. The control gate voltage only gives a start to the programming operation, but does not affect V_T shift.

Thus, the conventional hot electron injection programming method is not optimal

30 during the whole programming cycle. Indeed, if a constant voltage is applied to the control gate, the gate current is a strong function of the floating gate potential, as shown in Fig. 2.

Therefore, at the beginning of the programming cycle, the charging current is rather small; then, at some optimal potential (~1.2V in Fig. 2), the charging current is maximal. Then again, with the floating gate potential increase, the charging current becomes low again.

In accordance with the present invention, floating gate potential is always kept close

5   to (surfing on) the maximum of injection current (position 3, Fig. 2). In order to realize this during programming, the control gate is provided with a feedback correction as an additional voltage increase in order to compensate for the negative potential shift on the floating gate that is produced as a result of its charging in time.

Because the floating gate is isolated, its voltage and current cannot be monitored

10   directly. But, based on the fact of correlation between the injection current and the substrate current (Fig. 3), floating gate current is substituted with substrate current for the purpose of monitoring what the floating gate potential is. That is, in accordance with the invention, a feedback is implemented that increases control gate voltage to maintain substrate current at maximum.

15   The conventional programming method can make programming better (V_T shift larger) only by increasing the drain voltage (and accompanying increase of drain current). In contrast, the method disclosed herein also allows using control gate voltage to improve programming; the same programming effect may be achieved even with lower drain voltage and current.

20   In general, the feedback circuit can be implemented both by taking the informative potential from the whole memory cell array or by using only a single control memory cell to develop the potential for the separate array.

Practically, since the drain voltage is fixed, the disclosed method can be converged to the problem of supporting maximum substrate current through the cell during programming

25   by controlling the potential of the control gate.

The block diagram of the feedback circuit is presented in Figs. 4A and 4B. It contains sensor resistor in the substrate circuit and feedback circuit connected to the control gate bus.

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Although only specific embodiments of the present invention are shown and described herein, the invention is not to be limited by these embodiments. Rather, the scope of the invention is to be defined by these descriptions taken together with the attached claims and their equivalents.

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